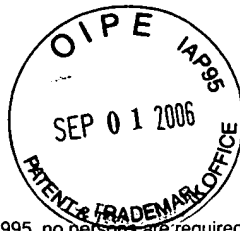


Doc Code: AP.PRE.REQ



PTO/SB/33 (07/05)
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PRE-APPEAL BRIEF REQUEST FOR REVIEW

Docket Number (Optional)

ITL.1004US (P16592)

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on August 29, 2006

Signature

Typed or printed
name

Stephanie Petreas

Application Number

10/630,287

Filed

July 30, 2003

First Named Inventor

Robert T. George, et al.

Art Unit

2181

Examiner

Niketa I. Patel

Applicant requests review of the final rejection in the above-identified application. No amendments are being filed with this request.

This request is being filed with a notice of appeal.

The review is requested for the reason(s) stated on the attached sheet(s).

Note: No more than five (5) pages may be provided.

I am the

☐

applicant/inventor.

☐

assignee of record of the entire interest.

See 37 CFR 3.71. Statement under 37 CFR 3.73(b) is enclosed.
(Form PTO/SB/96)

☒

attorney or agent of record.

Registration number 42,117

☐

attorney or agent acting under 37 CFR 1.34.

Registration number if acting under 37 CFR 1.34

Signature

Mark J. Rozman

Typed or printed name

512-418-9944

Telephone number

August 29, 2006

Date

NOTE: Signatures of all the inventors or assignees of record of the entire interest or their representative(s) are required. Submit multiple forms if more than one signature is required, see below*.

☒

*Total of 1 forms are submitted.

This collection of information is required by 35 U.S.C. 132. The information is required to obtain or retain a benefit by the public which is to file (and by the USPTO to process) an application. Confidentiality is governed by 35 U.S.C. 122 and 37 CFR 1.11, 1.14 and 41.6. This collection is estimated to take 12 minutes to complete, including gathering, preparing, and submitting the completed application form to the USPTO. Time will vary depending upon the individual case. Any comments on the amount of time you require to complete this form and/or suggestions for reducing this burden, should be sent to the Chief Information Officer, U.S. Patent and Trademark Office, U.S. Department of Commerce, P.O. Box 1450, Alexandria, VA 22313-1450. DO NOT SEND FEES OR COMPLETED FORMS TO THIS ADDRESS. SEND TO: Mail Stop AF, Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450.

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IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Applicants: Robert T. George, Et Al.

Serial No.: 10/630,287

Filed: July 30, 2003

For: Dynamically Partitioning
Pipeline Resources

§ Group Art Unit: 2181

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§ Examiner: Niketa I. Patel

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§ Atty. Dkt. No.: ITL.1004US (P16592)

§

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Alexandria, VA 22313-1450

REASONS FOR PRE-APPEAL BRIEF REQUEST FOR REVIEW

Sir:

Applicants seek pre-appeal review of the rejection of claims 1-10 and 17-30. It is respectfully submitted that the rejection to pending claims 1-10 and 17-30 is clearly erroneous and the burden of an appeal should be avoided.

Pending claims 1-10 and 17-30 stand rejected under 35 U.S.C. §102(e) over U.S. Patent No. 6,510,508 (Zuraski). The rejection is clearly erroneous, as Zuraski fails to teach each and every element of the claims, as required for a valid anticipation rejection. As to claim 1, Zuraski nowhere teaches either: (1) invalidating an entry of a filter if an update to the entry occurs during a context; or (2) flushing a portion of a pipeline resource coupled to the filter corresponding to an address space including the entry. In this regard, the Examiner refers to col. 9, lns. 48-61 and col. 11, lns. 14-20 of Zuraski to contend presence of the claimed invalidating of an entry. However, nowhere do these or any other portions of Zuraski anywhere teach that an entry in flush filter 40 is invalidated if an update to the entry occurs during a context. Instead, both of these portions only teach that a flush filter 40 asserts an Invalidate signal out to a translation lookaside buffer (TLB) 39. Nowhere do these or any other portions of Zuraski teach

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Stephanie Petreas

that such Invalidate signal invalidates an entry of the filter itself. Certainly, it nowhere teaches invalidating such an entry if an update to the entry occurs during a context.

Furthermore, nowhere does Zuraski anywhere teach flushing a portion of a pipeline resource corresponding to an address space including such an entry. In this regard, the Examiner refers to col. 13, lns. 3-11 of Zuraski. However, neither this nor any other portion of Zuraski teaches such flushing of a portion of a resource. Instead, all that Zuraski teaches is that upon the occurrence of certain events, flush filter 40 causes a flush of a TLB 39 *in its entirety*. That is, Zuraski, instead teaches:

In the embodiment shown, a flush of TLB may occur when filter circuit 403 asserts an Invalidate signal, *thereby invalidating all entries currently stored in TLB 39*.

Zuraski, col. 11, lns. 14-17 (emphasis added). Clearly, Zuraski contemplates that the *entire* TLB is flushed.

Nor does the passage of Zuraski cited in col. 13 anywhere teach flushing of a portion of a pipeline resource. Instead, this portion of Zuraski merely teaches:

As such, it is possible that some address translations loaded into the TLB from page table B are no longer valid. Consequently, *the TLB flush filter may allow a TLB flush* (shown here as a filtered flush) to occur following the next context switch.

Zuraski, col. 13, lns. 7-11 (emphasis added). Clearly, this does not teach the flushing of a portion; instead it is a full TLB flush. For at least these reasons, Zuraski does not teach flushing of only a portion of a pipeline resource, and certainly not a portion corresponding to an address space including an invalidated and updated entry of a filter. Accordingly, the rejection of claim 1 and its dependent claims is clearly erroneous.

Dependent claim 4 is further patentable, as Zuraski nowhere teaches comparing an address obtained from an external snoop to entries in the filter to determine if an update has occurred. In this regard, the Examiner refers to col. 10, lns. 1-17. All this portion of Zuraski teaches is that a flush filter 40 may receive a snoop request signal and a snoop address. However, Zuraski only teaches that this information is used “for searches of a region table.” Zuraski does not teach that an entry in a flush filter is invalidated based on a comparison of an address obtained from an external snoop.

Dependent claim 5 further recites flushing the portion of the pipeline resource via microcode. Zuraski does not teach that its flush operation is performed by microcode, contrary to the Examiner's contention. Instead, Zuraski merely teaches that an Invalidate signal is asserted to allow a flush of TLB 39. Zuraski, col. 9, lns. 53-55. To support the rejection of claim 5, the Office Action instead refers to an unrelated portion of Zuraski: col. 4, lns. 11-29. However, all this teaches is that an instruction cache includes tags as to whether an instruction is executed by invoking a microcode procedure. This portion has no relevance to the operation of the flush filter. As a result, there is no teaching of the claim 5 subject matter as recited in the claim, and accordingly claim 5 is patentable. *In re Bond*, 15 U.S.P.Q.2d 1566, 1567 (Fed. Cir. 1990) (every element of claim must be identically shown in a single reference).

As to independent claim 6, Zuraski nowhere teaches flushing a portion of entries of a pipeline resource if one of the portion is updated during a context. For claim 6, the Examiner simply refers to the same portions of Zuraski cited above with regard to claim 1. Because Zuraski nowhere teaches that its TLB has only a portion that is flushed if one of its entries is updated during a context, the rejection of claim 6 and its dependent claims is clearly erroneous.

As to independent claim 17, Zuraski nowhere teaches a pipeline resource having multiple address spaces that are each selectively flushable while the others are maintained. Instead, as described above, the TLB of Zuraski is flushed in its entirety. As to the recitation in the Office Action of claim 17 (*see* Final Office Action, p. 3), the Examiner ignores Applicants' prior amendment to claim 17. Because nothing in Zuraski teaches maintaining other address spaces in a pipeline resource while one address space is selectively flushed, claim 17 is patentable. Again the Examiner merely relies on col. 13, lns. 3-11 to contend such maintaining of entries. As discussed above, this portion of Zuraski, as with all others, teaches an entire flush of the TLB 39. Accordingly, the rejection of claim 17 and its dependent claims is clearly erroneous.

With regard to independent claim 21, Zuraski nowhere teaches either dynamic partitioning of a filter into multiple partitions, nor where such partitions each correspond to one of multiple address spaces. In this regard, there is no teaching anywhere in Zuraski of dynamic partitioning. Instead, the cited portion of Zuraski (i.e., col. 10, lns. 27-65) merely sets forth the fixed structure of the flush filter of Zuraski. That is, while the circuitry of the flush filter shown in FIG. 3 of Zuraski and described in col. 10 includes different components, Zuraski nowhere teaches that these components are dynamically partitioned. Instead, it appears the opposite is

true: the structures detailed in col. 10 of Zuraski are fixed and thus are not dynamically partitioned.

Further, Zuraski does not teach that these components are partitioned into partitions each corresponding to one of multiple address spaces. Instead, all that the Examiner cites in this regard is that a region table includes a CAM and a RAM to store addresses and tags. Nowhere however does Zuraski teach that such storage is partitioned so that each partition corresponds to only one of multiple address spaces. Accordingly, the rejection of claim 21 and its dependent claims is clearly erroneous. For at least similar reasons, so too is the rejection of claim 25 and its dependent claims clearly erroneous as Zuraski nowhere teaches the recited dynamic partitioning of a filter of a pipeline resource into multiple partitions each corresponding to one of multiple address spaces.

Dependent claim 23 further recites that each of the multiple partitions of a filter includes a fixed portion, and the filter further includes a dynamic portion. As contended support for this recited subject matter, the Examiner refers to a paragraph in the Summary of Invention (specifically lns. 36-51 of col. 2). Nowhere does this or any other portion of Zuraski anywhere teach that the flush filter 40 includes fixed partitions and a dynamic portion. Accordingly, for this further reason the rejection of claim 23 is clearly erroneous.

As to dependent claim 24, Zuraski further nowhere teaches allocating at least part of the dynamic portion to an application that has consumed the fixed portion of its partition. In fact, Zuraski appears to teach the opposite. That is, Zuraski teaches that when the region table of the flush filter 40 runs out of available resources an overflow signal is asserted, and that this overflow signal deactivates the flush filter 40. Zuraski, col. 10, lns. 49-65. Clearly, there is no teaching of allocating a dynamic portion if an application has consumed a fixed portion. Instead, an overflow occurs and the flush filter of Zuraski is simply deactivated. For this further reason the rejection of claims 24 and 27 is clearly erroneous.

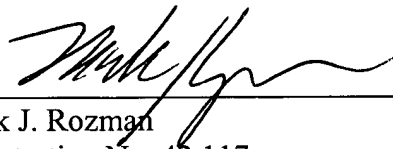
The rejection of independent claim 28 is clearly erroneous for similar reasons described above with regard to claim 17, as Zuraski nowhere teaches a pipeline resource with multiple address spaces each corresponding to one of multiple contexts, and where each of the address spaces is selectively flushable while the others are maintained. Accordingly, claim 28 and its dependent claims are patentable. This is especially so, as again the Examiner fails to acknowledge Applicants' amendments to claim 28.

Since these rejections are clearly violative of existing PTO policy, the need for an appeal should be avoided.

Respectfully submitted,

Date: _____

8/29/06



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